#22
3/4/04
SR

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	Kaplun et al.
Serial No.	09/783,626
Filing Date	February 14, 2001
Group Art Unit	2643
Examiner	Quoc D Tran
Attorney Docket No.	100.004US01

APPEAL BRIEF

Title: ALARM MECHANISM

Table of Contents

1. Introduction

On November 21, 2003, Appellants filed a notice of appeal from the final rejection of claims 1-34 set forth in the Office Action mailed July 22, 2003. Three copies of this Appeal Brief are hereby filed on February 24, 2004 and are accompanied by a fee in the amount of $330.00 as required under 37 C.F.R. §1.17(c).

This paper is also accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for filing the Appeal Brief, thereby moving the deadline for filing the brief from January 24, 2004 to February 24, 2004.

2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee ADC Telecommunications Israel, Ltd.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellants which will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1-34 are pending in the application and are the subject of this appeal. In office action mailed July 22, 2003, claims 1-22, 24-26 and 30-34 were finally rejected under 35 U.S.C. §102(b) claims 23 and 27-29 were finally rejected under 35 U.S.C. §103.

5. Status of Amendments

No amendment has been filed subsequent to the Final Office Action mailed July 22, 2003.

6. Summary of the Invention

In one embodiment, an alarm mechanism 102 is provided. The mechanism includes a hardware component 204, including first 208 and second 210 registers, the first register 208 adapted to store a value that indicates a change in state of at least one alarm and the second register 210 adapted to store current states of each of the at least one alarm. The mechanism also includes a software component 206, responsive to interrupt requests from the hardware component, adapted to read the first and second registers 208 and 210, respectively.

In another embodiment, an alarm mechanism 102 is provided. The mechanism includes at least one alarm. It also includes a first register 208, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm and a second register 210, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm.

In another embodiment, a method for monitoring alarm conditions, Fig. 3, is provided. The method includes receiving an indication of a change in state of an alarm 304. The method also includes a recording the change in state of the alarm in a first register 308. The method also includes recording the current state of the changed alarm in a second register 310 and further includes generating an interrupt 312.

7. Issues Presented for Review

The first issue presented in this Appeal is whether the Examiner erred in rejecting claims 1-22, 24-26 and 30-34 under 35 U.S.C. §102(b), as being anticipated by Tyburski et al. (U.S. Patent 5,495,470) (referred to herein as "Tyburski"). A second issue presented in this Appeal is whether the Examiner erred in rejecting claims 27-29 as being unpatentable over Tyburski in view of Gradl et al. (U.S. Patent 6,381,269) (referred to herein as "Gradl"). A third issue presented in this Appeal is whether the Examiner erred in rejecting claim 23 as being unpatentable over Tyburski in view of Anand (U.S. Patent 5,426,688) (referred to herein as

"Anand").

8. Grouping of Claims

Each of claims 1-34 stands or falls on their own merits for reasons detailed below. Each of the claims is patentably distinct for the reasons detailed below.

9. Arguments

A. Rejections of claims 1-22, 24-26 and 30-34 under 35 U.S.C. §102 (b)

1. The Applicable Law

35 U.S.C. §102 provides in relevant part:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbi* test, i.e., identity of terminology is not required. *In re Bond*, 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). *See*, M.P.E.P. 2131.

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberyl-Clark Corp.,* 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating

subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

2. 35 U.S.C. § 102(b) rejection analysis

The Examiner finally rejected claims 1-22, 24-26 and 30-34 under 35 U.S.C. §102(b) as being anticipated by Tyburski.

Claim 1

Claim 1 is directed to an alarm mechanism. The alarm mechanism includes a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm. The mechanism also includes a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

In support of this rejection, the final Office Action states that Tyburski et al recites:

"Tyburski et al. teach an alarm mechanism, comprising: a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm; and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36)."

> "The access system...continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and...intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control.*** In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates***. Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170. The access system*** 170 integrates monitor, access, and test functions into one system

having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC254.*** The sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of utility***...***The software for the access system*** 170 also comprises ***a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface*** 171 (FIG.4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250. PM statistics are accumulated and stored in on-board semiconductor memory at state 395.*** Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, and alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS...If no threshold is reached, or the alarm/event message has been sent, the PM process 393 terminates.*** As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see. Col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38, col. 20 lines 22-36)." Final Office Action at p.9.

Applicant respectfully asserts that Tyburski fails to teach or suggest the method of claim 1. In particular, Tyburski fails to teach a hardware component, including first and second registers wherein the first register is adapted to store **a value that indicates a change in state** of at least one alarm. (See pg. 4, lines 9-12, 15-19; pg. 5, lines 6-12; pg. 6, lines 11-16 of Detailed Description and Fig. 2 & 3). Further, Tyburski fails to teach the second register adapted to store current states of each of the at least one alarm as in claim 1. In addition, the Tyburski does not teach or suggest a software component, **responsive to interrupt requests** (312) from the hardware component, adapted to read first and second registers as found in claim 1. (See pg. 6, lines 22-23 of Detailed Description and Fig. 3). As a result Tyburski does not anticipate claim 1.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 1 of the present application under 35 USC § 102(b).

Claims 2-6

Claims 2-6 depend from claim 1 and therefore the arguments set forth above with respect to claim 1 also apply to these claims. Claims 2-6 are allowable for at least the reasons provided above with respect to claim 1.

Claim 7, 14 and 19

Claim 7 is directed to an alarm mechanism. The mechanism includes at least one alarm; a first register, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm; and a second register, responsive to at least one alarm, and adapted to store current states of each of the at least one alarm.

In support of this rejection, the final Office Action states that Tyburski et al recites:

> "The access system...continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and...intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control.*** In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates***. Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170. The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC254.*** The sixteen bit

words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of utility***...***The software for the access system*** 170 also comprises ***a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface*** 171 (FIG.4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250. PM statistics are accumulated and stored in on-board semiconductor memory at state 395.*** Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, and alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS...If no threshold is reached, or the alarm/event message has been sent, the PM process 393 terminates.*** As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see. Col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36)." Final Office Action at p.11.

As provided in the arguments with respect to claim 1, the Applicant respectfully asserts that Tyburski fails to teach the method of claim 7. In particular, Tyburski fails to teach an alarm mechanism including a first register, responsive to the at least one alarm, and adapted to store **a value that indicates a change in state** of at least one alarm as found in claim 7. (See pg. 4, lines 9-12, 15-19; pg. 5, lines 6-12; pg. 6, lines 11-16 of Detailed Description and Fig. 2 & 3) In addition, Tyburski does not teach or suggest a second register, responsive to at least one alarm, and adapted to store current states of each of the at least one alarm as found in claim 7. As a result, Tyburski does not anticipate claim 7. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 7 of the present application under 35 USC § 102(b).

Claims 8-13

Claims 8-13 depend from claim 7 and therefore the arguments set forth above with respect to claim 7 also apply to these claims. Claims 8-13 are allowable for at least the reasons provided above with respect to claim 7.

Claim 14

Claim 14 is directed to a method for monitoring alarm conditions. The method includes receiving an indication of a change in state of an alarm, recording the change in state of the alarm in a first register, recording the current state of the changed alarm in a second register, and generating an interrupt.

The Office action states "Consider claim 14, Tyburski et al. teach a method for monitoring alarm conditions, the method comprising: receiving an indication of a change in state of an alarm; recording the change in state of the alarm in a first register; recording the current state of the changed alarm in a second register; and generating an interrupt (col. 8 lines 30-52; col. 9 line 56-col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36)." Applicant respectfully traverses this rejection and has carefully reviewed Tyburski and does not find that Tyburski teaches or suggests the method of claim 14.

As provided in the arguments with respect to claim 1, the Applicant respectfully asserts that Tyburski fails to teach the method of claim 14. Applicant respectfully asserts that Tyburski fails to teach the method for monitoring alarm conditions as found in claims 14-18. In particular, Tyburski does not teach a method for monitoring alarm conditions including "receiving an indication of a change in state of an alarm". In addition, Tyburski fails to teach or suggest "recording the change in state of the alarm in a first register". (See pg. 4, lines 9-12, 15-19; pg. 5, lines 6-12; pg. 6, lines 11-16 of Detailed Description and Fig. 2 & 3). As a result, claim 14 is not anticipated by Tyburski and the Examiner has erred in the rejection of claim 14 and it should be allowed.

Claim 15-18

Claims 15-18 depend from claim 14 and therefore the arguments set forth above with respect to claim 14 also apply to these claims. Claims 15-18 are allowable for at least the reasons provided above with respect to claim 14.

Claim 19

Claim 19 is directed to a telecommunications system. The system including at least one access device having a plurality of ports adapted to couple to a plurality of subscriber lines, a plurality of line cards disposed in the at least one assess device and providing the plurality of ports, and a monitoring circuit disposed in the access device. The monitoring circuit adapted to monitor for alarm conditions for the at least one access device. The system further includes an alarm mechanism, communicatively coupled to the monitoring circuit, the alarm mechanism including a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of the at least one alarm and the second register adapted to store current states of each of the at least one alarm, and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

The Office action states: "Consider claim 19, Tyburski et al. teach a telecommunications system, comprising: at least one access device having a plurality of ports adapted to couple to a plurality of subscriber lines; a plurality of lie cards disposed in the at least one access device and providing the plurality of ports; a monitoring circuit disposed in the access device, the monitoring circuit adapted to monitor for alarm conditions for the at least one access device; and an alarm mechanism, communicatively coupled to the monitoring circuit (col. 8 lines 30-52; col. 9 line 56- col. 11 line 43; col. 14 lines 19-38), the alarm mechanism including: hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm, and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 8 lines 30-52; col. 9 line 56- col.11 line 43; col. 14 lines 19-38; col. 20 lines 22-36)."

As provided in the arguments with respect to claim 1, the Applicant respectfully asserts that Tyburski fails to teach the method of claim 19. In particular, Tyburski fails to teach "a

telecommunications system including a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm" as found in claim 19. (See pg. 4, lines 9-12, 15-19; pg. 5, lines 6-12; pg. 6, lines 11-16 of Detailed Description and Fig. 2 & 3). As a result, claim 19 is not anticipated by Tyburski and the Examiner has erred in the rejection of claim 19 and it should be allowed.

Claim 20-26

Claims 20-26 depend from claim 19 and therefore the arguments set forth above with respect to claim 19 also apply to these claims. Claims 20-26 are allowable for at least the reasons provided above with respect to claim 19.

Claim 30

Claim 30 is directed to a method for monitoring alarm conditions in an access device. The method includes monitoring a plurality of serial lines on a back plane of the access device, when successive cells have corrupted synchronization patterns, generating an alarm. The method further includes receiving the alarm, recording a change in state of an alarm in a first n-bit register, recording the current state of the changed alarm in a second n-bit register, and generating an interrupt for a software component to read the first and second n-bit registers.

The Office Action states "Consider claim 30, Tyburski et al. teach a method for monitoring alarm conditions in an access device, the method comprising: monitoring a plurality of serial lines on a backplane of the access device (col. 13 line 55-col. 14 line 7; col. 14 line 61-col.15 line 45); when successive cells have corrupted synchronization patterns, generating an alarm; receiving the alarm; recording a change in state of an alarm in a first n-bit register; recording the current state of the changed alarm in a second n-bit register; and generating an interrupt for a software component to read the first and second n-bit registers (col. 8 lines 30-52; col. 9 line 56- col.11 line 43; col. 14 lines 19-38; col. 20 lines 22-36)."

In support of this rejection, the final Office Action states that Tyburski et al recites:

"The access system...continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and...intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control.*** In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates***. Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170. The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC254.*** The sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of utility...A crosspoint switch array 278 is provided as the interface between the DAI 250 and the DS2 links 282 on the backplane.*** In this manner any of the seven DS2 signals from the DAI 250 can be connected to any of the seven DS2 links 282 on the backplane...the DS2 data coming from the DAI 250 is fed through inverting buffers 280 and out onto the backplane. Both the DS2 clock and frame signals coming from the DAI 250 are sent through 7x7 crosspoint arrays 278 and fed through non-inverting buffers 280' (not shown) and out to the backplane...***The software for the access system*** 170 also comprises **a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface** 171 (FIG. 4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250. PM statistics are accumulated and stored in on-board semiconductor memory at state 395.*** Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, an alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS...If no threshold is reached, or the alarm/event message has been***

sent, the PM process 393 terminates. As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 13 line 55 – col. 14 line 7; col. 14 lines 19-38; col. 14 line 61 – col. 15 line 45; col. 20 lines 22-36).

As provided in the arguments with respect to claim 1, the Applicant respectfully asserts that Tyburski fails to teach a method of monitoring alarm conditions in an access device as found in claim 30. In particular, Tyburski fails to teach or suggest the method comprising "recording a change in state of an alarm in a first n-bit register" as found in claim 30. (See pg. 4, lines 9-12, 15-19; pg. 5, lines 6-12; pg. 6, lines 11-16 of Detailed Description and Fig. 2 & 3) As a result, claim 30 is not anticipated by Tyburski and the Examiner has erred in the rejection of claim 30 and it should be allowed.

Claim 31-34

Claims 31-34 depend from claim 30 and therefore the arguments set forth above with respect to claim 30 also apply to these claims. Claims 31-34 are allowable for at least the reasons provided above with respect to claim 30.

B. Rejection of claims 23 and 27-29 under 35 U.S.C. §103(a)

1. Applicable Law

35 U.S.C.§ 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

To establish a case of *prima facie* obviousness, three basic criteria must be met. First,

there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based in the applicant's disclosure. *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir 1991). MPEP § 2143 - § 2143.03.

2. 35 U.S.C. § 103(a) Rejection Analysis

The Examiner finally rejected claims 27-29 under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 5,495,470 (Tyburski) in view of US Patent No. 6,381,269 (Gradl). Claim 23 is also rejected as being unpatentable over Tyburski in view of US Patent No. 5,426,688 (Anand). Applicant respectfully asserts that the Examiner erred in making these rejections and that the claims are allowable.

Claim 27

Claim 27 is directed to an alarm mechanism for a telecommunications access device. The mechanism includes at least one alarm associated with each of a plurality of serial low voltage differential signal (LVDS) lines of the access device; a first n-bit register, responsive to the at least one alarm and adapted to store a value that indicates a change in state of at least one alarm; a second n-bit register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm; and wherein corresponding bits of the first and second n-bit registers are associated with a corresponding alarm and a corresponding LVDS line.

The Office Action states "Consider claim 27, Tyburski et al. teach an alarm mechanism for a telecommunications access device, comprising: at least one alarm associated with each of a plurality of serial lines of the access device; a first n-bit register, responsive to the at least one alarm and adapted to store a value that indicates a change in state of the at least one alarm; a

second n-bit register, responsive to the at least one alarm, and adapted to store current states of each of that at least one alarm; and wherein corresponding bits of the first and second n-bit registers are associated with a corresponding alarm and a corresponding line (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36

In support of this rejection, the final Office Action states that Tyburski et al recites:

"The access system...continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and...intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control.*** In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates***. Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170. The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC254.*** The sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of utility...A crosspoint switch array 278 is provided as the interface between the DAI 250 and the DS2 links 282 on the backplane.*** In this manner any of the seven DS2 signals from the DAI 250 can be connected to any of the seven DS2 links 282 on the backplane...the DS2 data coming from the DAI 250 is fed through inverting buffers 280 and out onto the backplane. Both the DS2 clock and frame signals coming from the DAI 250 are sent through 7x7 crosspoint arrays 278 and fed through non-inverting buffers 280' (not shown) and out to the backplane...***The software for the access system*** 170 also comprises **a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface** 171 (FIG. 4). The process 393 begins at

state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250. PM statistics are accumulated and stored in on-board semiconductor memory at state 395.*** Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, an alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS...If no threshold is reached, or the alarm/event message has been sent, the PM process 393 terminates.*** As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 13 line 55 – col. 14 line 7; col. 14 lines 19-38; col. 14 line 61 – col. 15 line 45; col. 20 lines 22-36).

As provided with respect to claim 1, the Applicant respectfully asserts that Tyburski fails to teach an alarm mechanism as found in claim 30. In particular, Tyburski and Gradl fails to teach or suggest the method comprising "a first n-bit register, responsive to the at least one alarm and adapted to store a value **that indicates a change in state** of the at least one alarm" as found in claim 30. (See pg. 4, lines 9-12, 15-19; pg. 5, lines 6-12; pg. 6, lines 11-16 of Detailed Description and Fig. 2 & 3) As a result, Tyburski alone or in combination does not teach or suggest the apparatus of claim 30 and should be allowed. Thus, the Examiner has failed to establish prima facie case of obviousness with respect to claims 27 and it should be allowed.

Claim 28-29

Claims 28-29 depend from claim 27 and therefore the arguments set forth above with respect to claim 30 also apply to these claims. Claims 28-29are allowable for at least the reasons provided above with respect to claim 27

Claim 23

Claim 23 depends from allowable claim 19 and therefore the arguments set forth above with respect to claim 23 also apply to claim 19. As a result, for at least the reasons provided above claim 23 should also be allowable.

10. Summary

Appellants have set forth reasons why the Examiner is incorrect in maintaining the rejections of the pending claims. Specifically, the Examiner has failed to set forth a prima facie case of anticipation or obviousness. Tyburski, Gradl and Anand either alone or in combination do not teach all of the limitations in the pending independent and dependant claims. Appellant respectfully submits that, for the above reasons, Claims 1-34 are allowable over the cited art. Therefore, reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,

Date: 24 February 2004

Laura A. Ryan
Reg. No. 49,055

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T 612 332-4720
F 612 332-4731

Appendix 1
The Claims on Appeal

1. An alarm mechanism, comprising:

a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm; and

a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

2. The alarm mechanism of claim 1, wherein the first and second registers comprise first and second n-bit registers for monitoring n alarms.

3. The alarm mechanism of claim 1, and further including a monitoring circuit adapted to monitor serial lines on the backplane of an access device of a telecommunications network to detect alarm conditions and to report alarm conditions to the hardware component.

4. The alarm mechanism of claim 1, wherein the second register is adapted to store a first value for a first state and second value for a second state.

5. The alarm mechanism of claim 4, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

6. The alarm mechanism of claim 1, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator.

7. An alarm mechanism, comprising:

at least one alarm;

a first register, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm; and

a second register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm.

8. The alarm mechanism of claim 7, wherein the at least one alarm comprises an alarm for a serial line on the backplane of an access device.

9. The alarm mechanism of claim 7, wherein the first and second registers comprise first and second n-bit registers for monitoring n alarms.

10. The alarm mechanism of claim 7, and further including a monitoring circuit adapted to monitor serial lines on the backplane of an access device of a telecommunications network to detect alarm conditions and to report alarm conditions to the hardware component.

11. The alarm mechanism of claim 7, wherein the second register is adapted to store a first value for a first state and a second value for a second state.

12. The alarm mechanism of claim 11, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

13. The alarm mechanism of claim 7, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator.

14. A method for monitoring alarm conditions, the method comprising:
receiving an indication of a change in state of an alarm;
recording the change in state of the alarm in a first register;
recording the current state of the changed alarm in a second register; and
generating an interrupt.

15. The method of claim 14, wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm condition in a serial line on a backplane of an access device.

16. The method of claim 14, wherein recording the change in state comprises recording a first logic value in a bit location of the first register.

17. The method of claim 14, wherein recording the current state comprises recording a first logic value in a bit location of the second register.

18. The method of claim 14, wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm condition when at least two cells are received on communication line with corrupted synchronization patterns.

19. A telecommunications system, comprising:
at least one access device having a plurality of ports adapted to couple to a plurality of subscriber lines;
a plurality of line cards disposed in the at least one access device and providing the plurality of ports;
a monitoring circuit disposed in the access device, the monitoring circuit adapted to monitor for alarm conditions for the at least one access device; and

an alarm mechanism, communicatively coupled to the monitoring circuit, the alarm mechanism including:

a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm, and

a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

20. The telecommunications system of claim 19, wherein the access device comprises a multimedia channel bank.

21. The telecommunications system of claim 19, wherein the access device comprises a digital loop carrier.

22. The telecommunications system of claim 19, wherein the monitoring circuit comprises a monitoring circuit that monitors serial lines on the backplane of the access device.

23. The telecommunications system of claim 19, wherein the line cards comprise at least one of Plain Old Fashion Telephone Service (POTS), digital subscriber line (DSL), and Integrated Services Digital Network (ISDN).

24. The telecommunications system of claim 19, wherein the first and second registers comprise first and second n-bit registers.

25. The telecommunications system of claim 19, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

26. The telecommunications system of claim 19, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm.

27. An alarm mechanism for a telecommunications access device, comprising:

at least one alarm associated with each of a plurality of serial low voltage differential signal (LVDS) lines of the access device;

a first n-bit register, responsive to the at least one alarm and adapted to store a value that indicates a change in state of the at least one alarm;

a second n-bit register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm; and

wherein corresponding bits of the first and second n-bit registers are associated with a corresponding alarm and a corresponding LVDS line.

28. The alarm mechanism of claim 27, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

29. The alarm mechanism of claim 27, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator.

30. A method for monitoring alarm conditions in an access device, the method comprising:

monitoring a plurality of serial lines on a back plane of the access device;

when successive cells have corrupted synchronization patterns, generating an alarm;

receiving the alarm;

recording a change in state of an alarm in a first n-bit register;

recording the current state of the changed alarm in a second n-bit register; and

generating an interrupt for a software component to read the first and second n-bit registers.

31. The method of claim 30, wherein receiving an alarm indicator comprises receiving an indication of an alarm condition in a serial line on the backplane of an access device.

32. The method of claim 30, wherein recording a change in state comprises recording a first logic value in a bit location of the first n-bit register.

33. The method of claim 30, wherein recording the current state comprises recording a first logic value in a bit location of the second n-bit register.

34. The method of claim 30, wherein receiving the alarm comprises receiving an indication of an alarm condition when at least two cells are received on communication line with corrupted synchronization patterns.